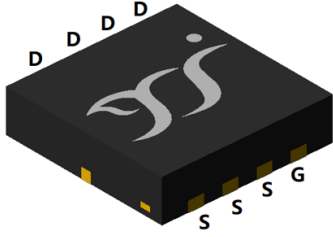
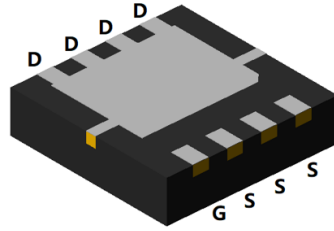


## N-Channel Enhancement Mode Field Effect Transistor

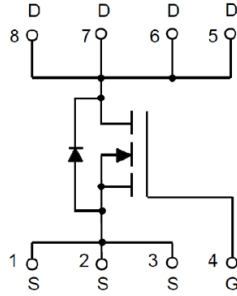


Top View



Bottom View

**DFN3333-8L**



### Product Summary

- $V_{DS}$  30V
- $I_D$  50A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) <6.0 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) <7.0 mohm
- 100% EAS Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	30	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	12	A
	$T_A=100^\circ C$		7	
	$T_C=25^\circ C$		50	
	$T_C=100^\circ C$		31	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	190	A
Total Power Dissipation	$T_A=25^\circ C$	$P_D$	2	W
	$T_A=100^\circ C$		0.8	
	$T_C=25^\circ C$		35	
	$T_C=100^\circ C$		14	
Single Pulse Avalanche Energy <sup>B</sup>		$E_{AS}$	128	mJ
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	3.6	$^\circ C/W$
Thermal Resistance Junction-to- Ambient <sup>C</sup>		$R_{\theta JA}$	60	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ50N03A	F1	Q50N03	5000	10000	100000	13" reel



# YJQ50N03A

RECOMMEND  
YJQ65N03A  
FOR NEW DESIGN

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =15A		4.9	6.0	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =15A		5.9	7.0	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				50	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		2504		pF
Output Capacitance	C <sub>oss</sub>			323		
Reverse Transfer Capacitance	C <sub>rss</sub>			283		
Gate resistance	R <sub>g</sub>	F= 1MHz		1.5		Ω
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		54		nC
Gate-Source Charge	Q <sub>gs</sub>			26		
Gate-Drain Charge	Q <sub>gd</sub>			8.5		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>r</sub> =15A, di/dt=100A/us		10.2		ns
Reverse Recovery Time	t <sub>rr</sub>			15		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =2A R <sub>GEN</sub> =3Ω		11		ns
Turn-on Rise Time	t <sub>r</sub>			20		
Turn-off Delay Time	t <sub>D(off)</sub>			41		
Turn-off fall Time	t <sub>f</sub>			25		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=24V, V<sub>G</sub>=10V, L=1mH, I<sub>AS</sub>=16A

C. The value of RθJA is measured with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



## Typical Performance Characteristics

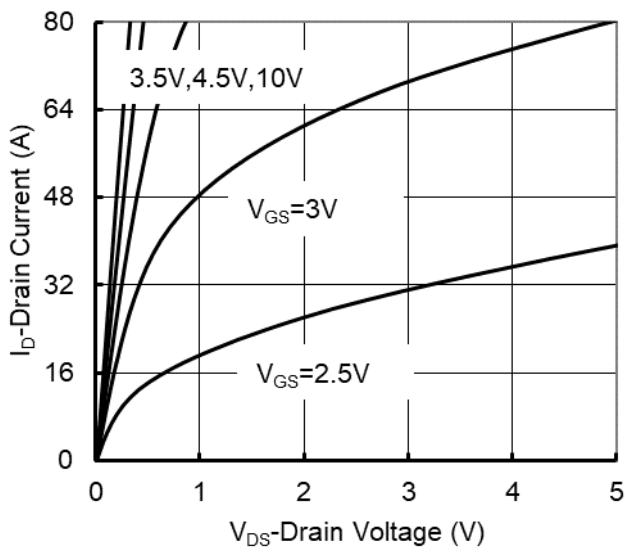


Figure1. Output Characteristics

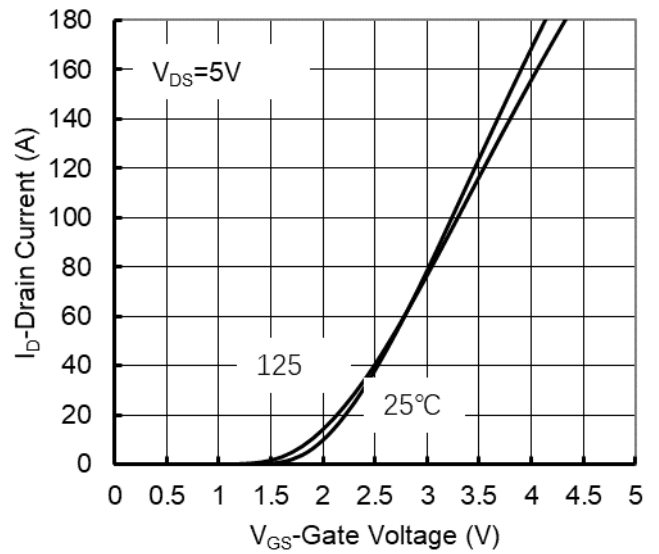


Figure2. Transfer Characteristics

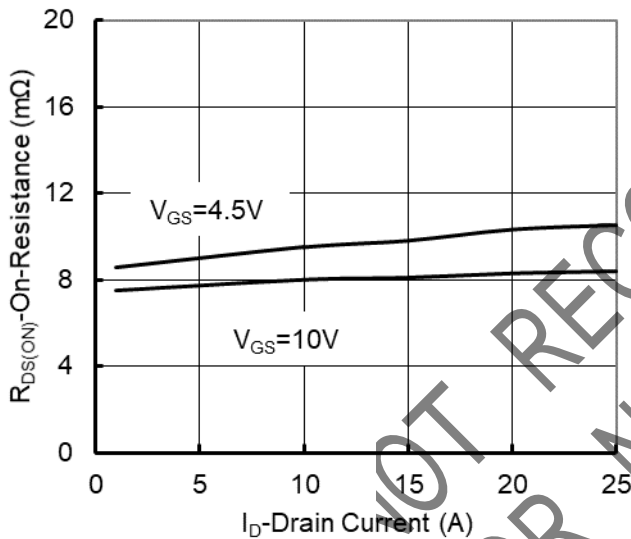


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

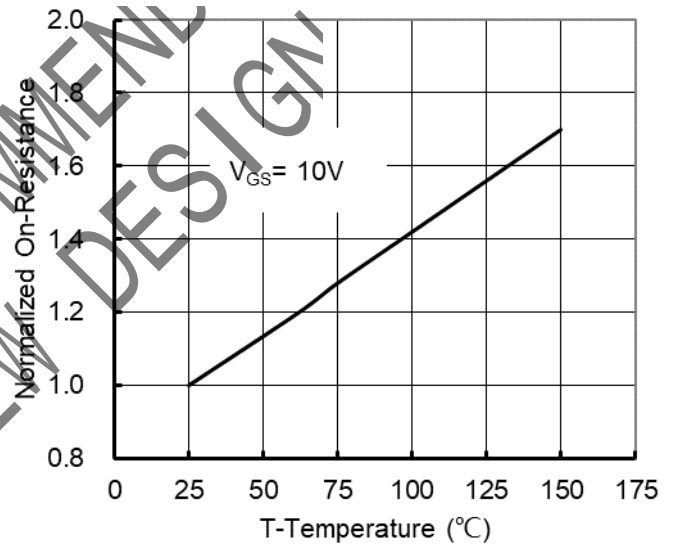


Figure 4: On-Resistance vs. Junction Temperature

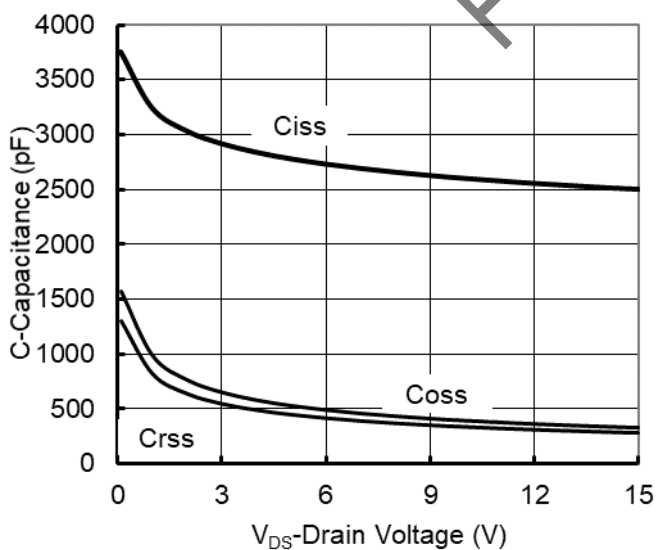


Figure5. Capacitance Characteristics

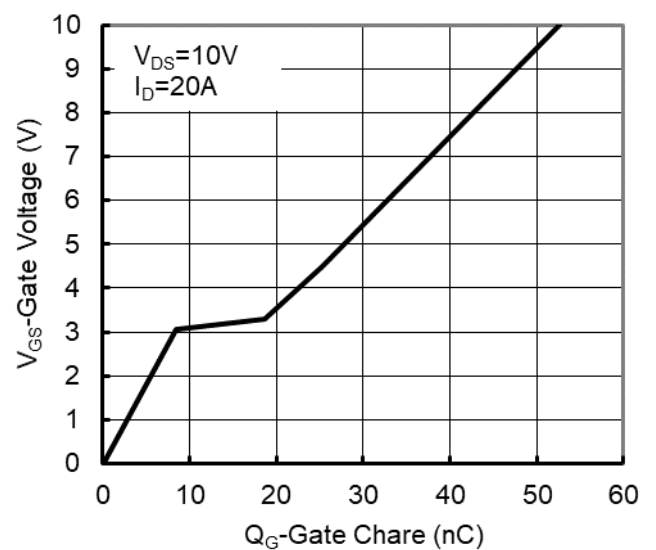


Figure6. Gate Charge

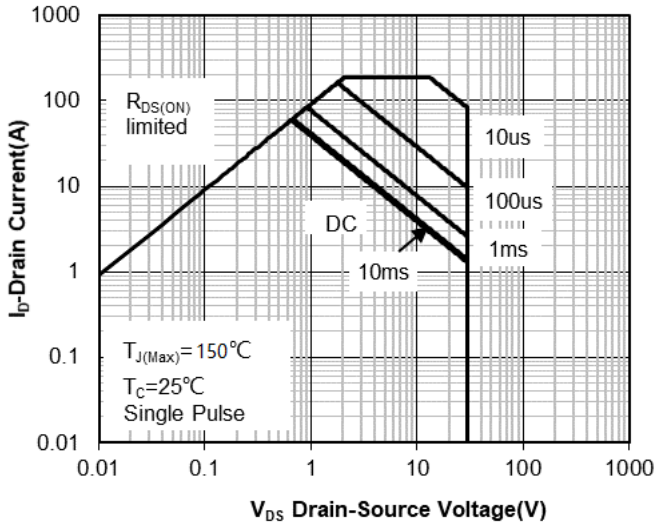


Figure7. Safe Operation Area

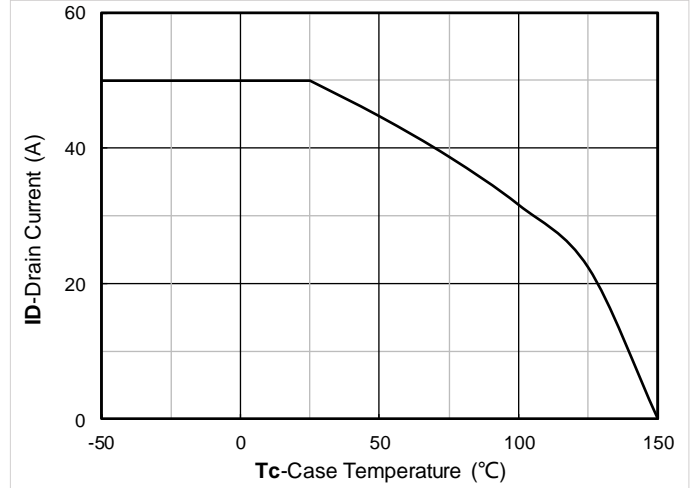


Figure8. Maximum Continuous Drain Current vs Case Temperature

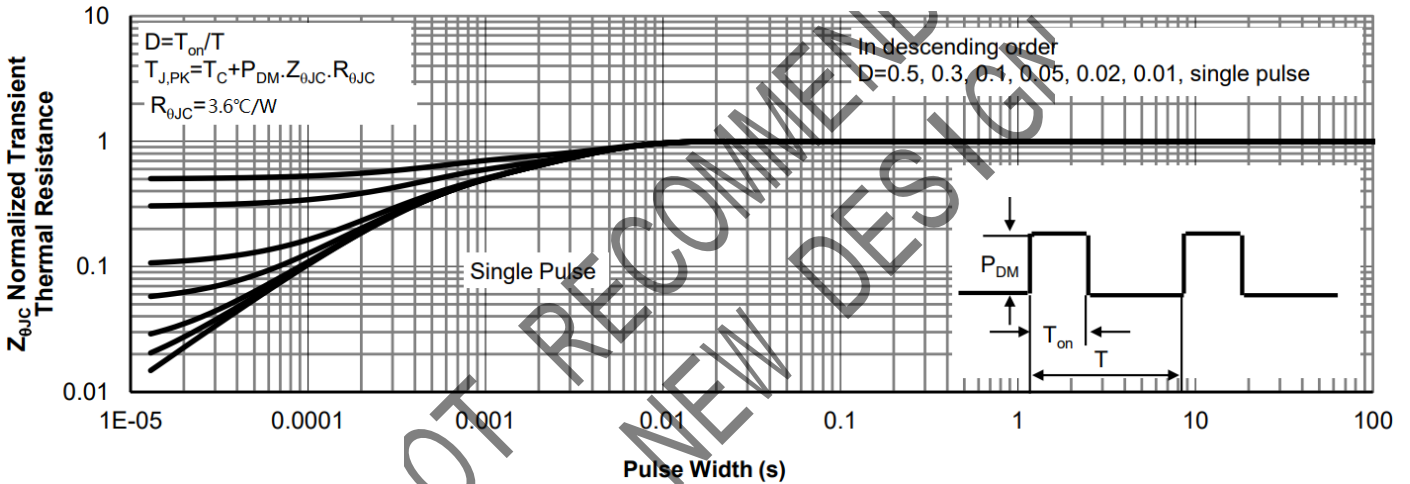
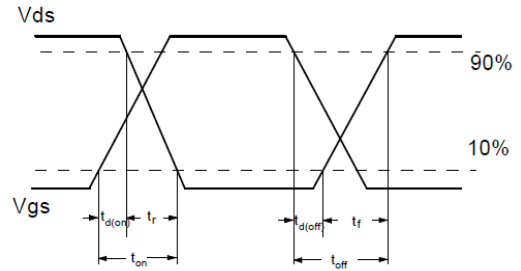
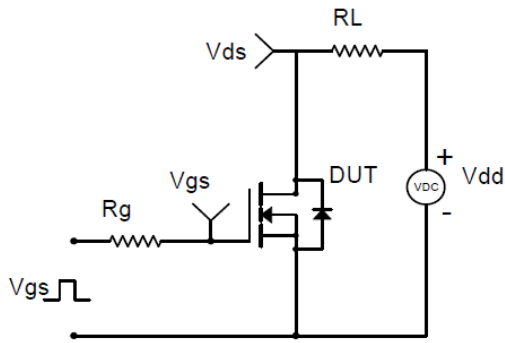
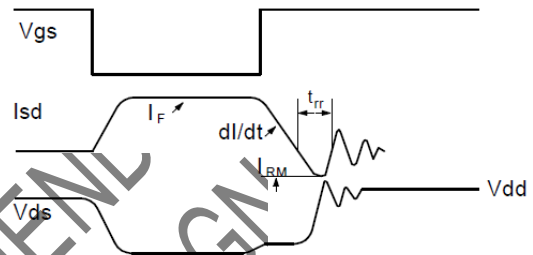
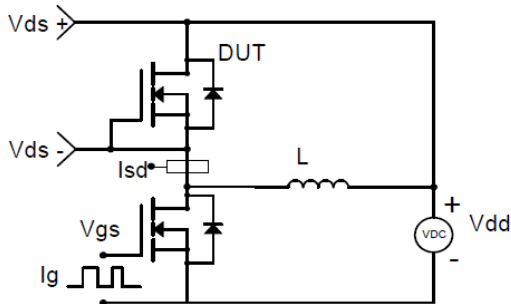


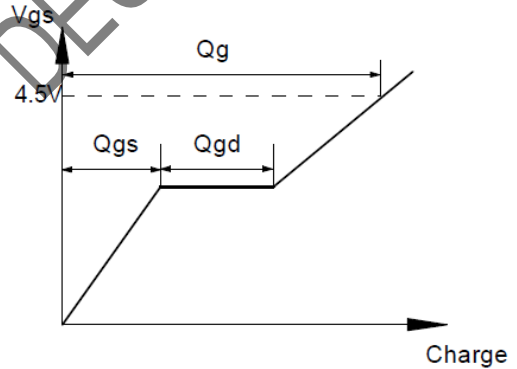
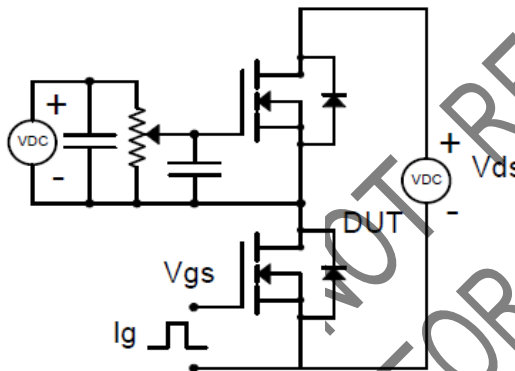
Figure9. Normalized Maximum Transient Thermal Impedance



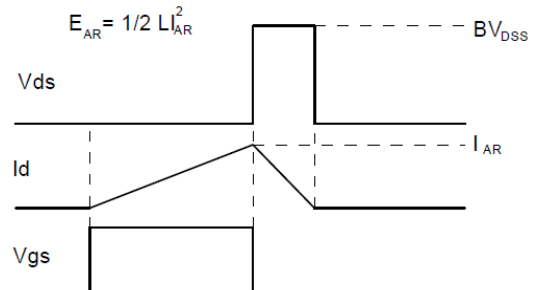
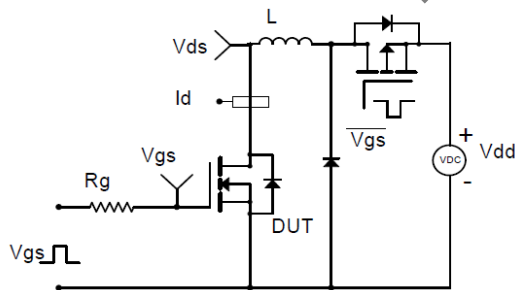
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



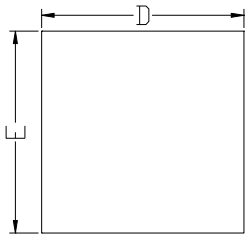
**Gate Charge Test Circuit & Waveform**



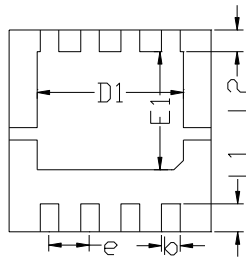
**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



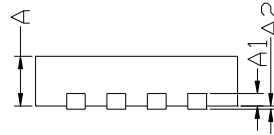
■DFN3333-8L Package information



Top View  
正面视图

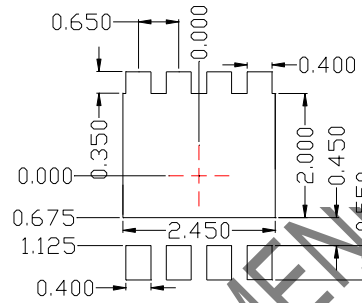


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

- Note:
1. Controlling dimension: in millimeters.
  2. General tolerance:  $\pm 0.10$ mm.
  3. The pad layout is for reference purposes only.

NOT RECOMMENDED FOR NEW DESIGN



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