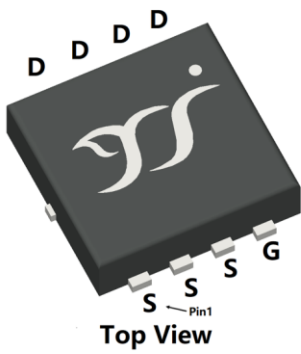
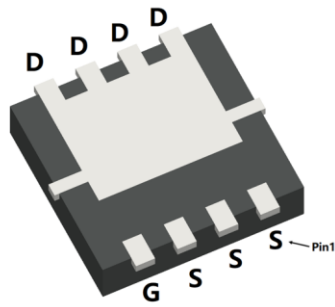


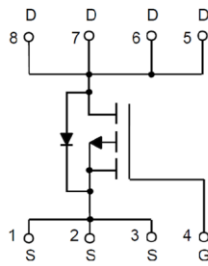
## P-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View



PDFN3333-8L

### Product Summary

- $V_{DS}$  -100V
- $I_D$  -8A
- $R_{DS(ON)}$  (at  $V_{GS}=-10V$ ) <200m $\Omega$
- $R_{DS(ON)}$  (at  $V_{GS}=-4.5V$ ) <235m $\Omega$
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

### ■ Absolute Maximum Ratings ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Limit	Unit	
Drain-source Voltage			$V_{DS}$	-100	V	
Gate-source Voltage			$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$	$I_D$	-2	A	
		$T_A=100^\circ\text{C}$		-1.2		
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ\text{C}$		-8		
		$T_C=100^\circ\text{C}$		-5		
Pulsed Drain Current	$T_C=25^\circ\text{C}$ , $t_p=100\mu\text{s}$		$I_{DM}$	-25	A	
Avalanche energy			$V_G=-10V$ , $R_G=25\Omega$ , $L=0.5\text{mH}$ , $I_{AS}=-10.5A$	EAS	27.56	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$	$P_D$	1.78	W	
		$T_A=100^\circ\text{C}$		0.71		
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^\circ\text{C}$		29.7		
		$T_C=100^\circ\text{C}$		11.9		
Junction and Storage Temperature Range			$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$	

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	56	70	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	3.5	4.2	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ200P10AJ	F1	Q200P10	5000	10000	100000	13" reel



# YJQ200P10AJ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-100V, V <sub>GS</sub> =0V	-	-	-1	μA
		V <sub>DS</sub> =-100V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	-100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.1	-1.6	-2.1	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5A	-	155	200	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A	-	170	235	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-5A, V <sub>GS</sub> =0V	-	-	-1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	18	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	-8	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-50V, V <sub>GS</sub> =0V, f=1MHz	-	1370	-	pF
Output Capacitance	C <sub>oss</sub>		-	34	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	29	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-50V, I <sub>D</sub> =-0.5A	-	18	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	2	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =-0.5A, di/dt=100A/us	-	23.7	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	20.8	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-50V, I <sub>D</sub> =-0.5A R <sub>GEN</sub> =2.7Ω	-	6.5	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	23.6	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	131	-	
Turn-off fall Time	t <sub>f</sub>		-	133	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R<sub>θJA</sub> is measured with the device mounted on the 40mm\*40mm\*1.1mm single layer FR-4 PCB board with 1 in<sup>2</sup> pad of 2oz. Copper, in the still air environment with T<sub>A</sub> =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).

## Typical Electrical and Thermal Characteristics Diagrams

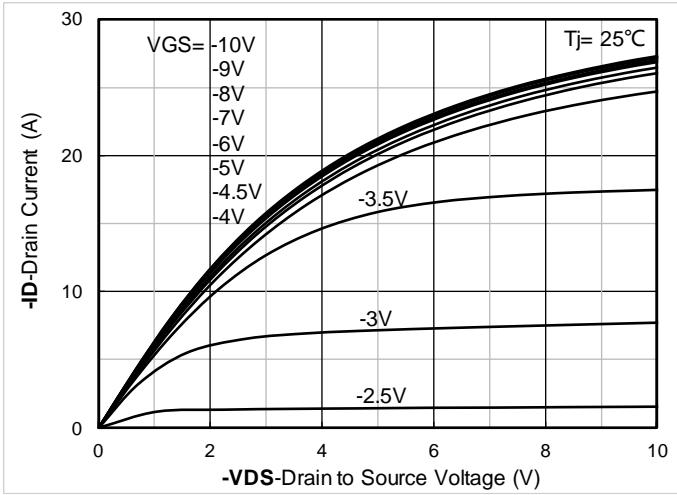


Figure 1. Output Characteristics

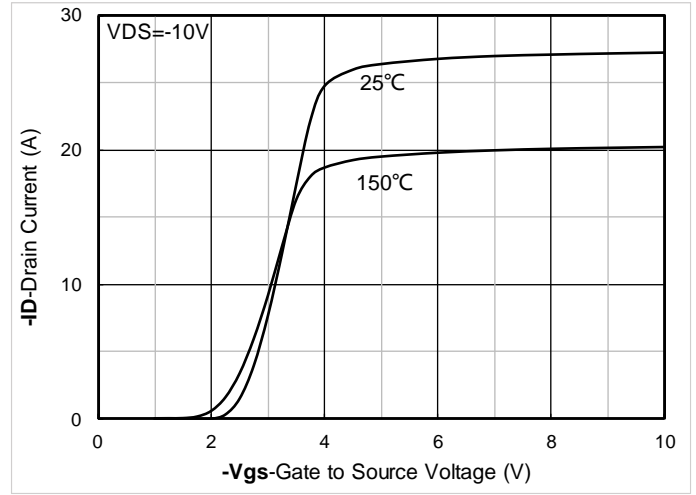


Figure 2. Transfer Characteristics

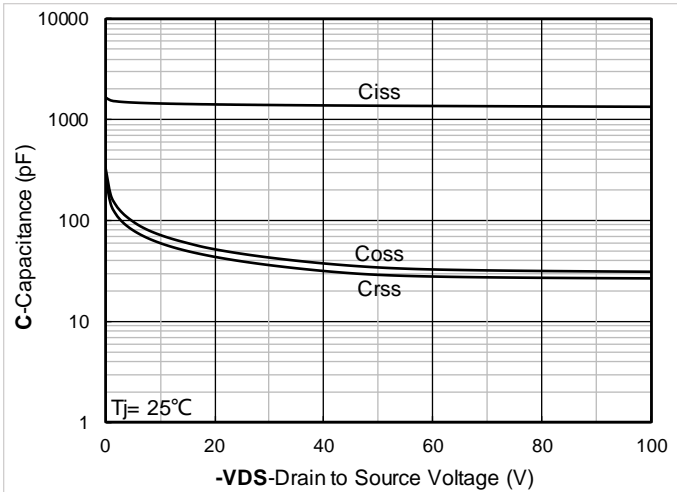


Figure 3. Capacitance Characteristics

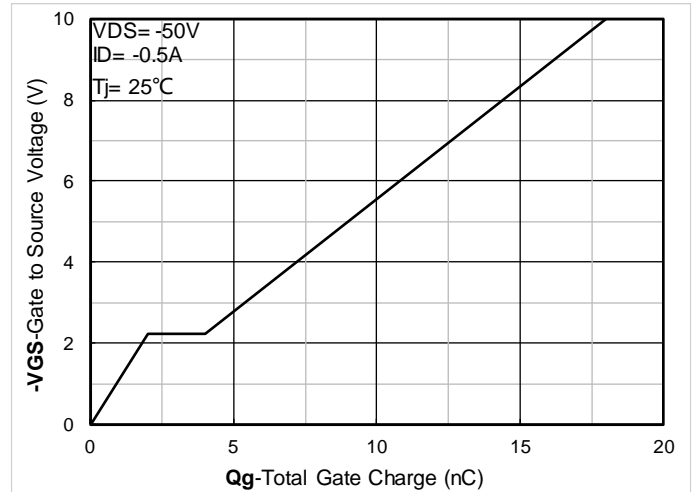


Figure 4. Gate Charge

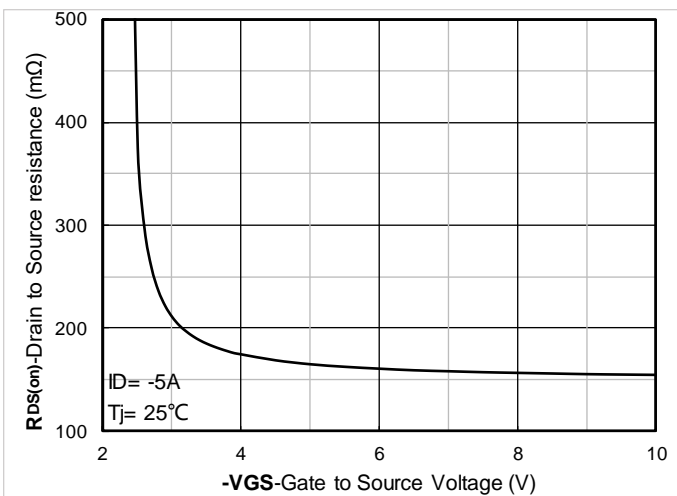


Figure 5. On-Resistance vs Gate to Source Voltage

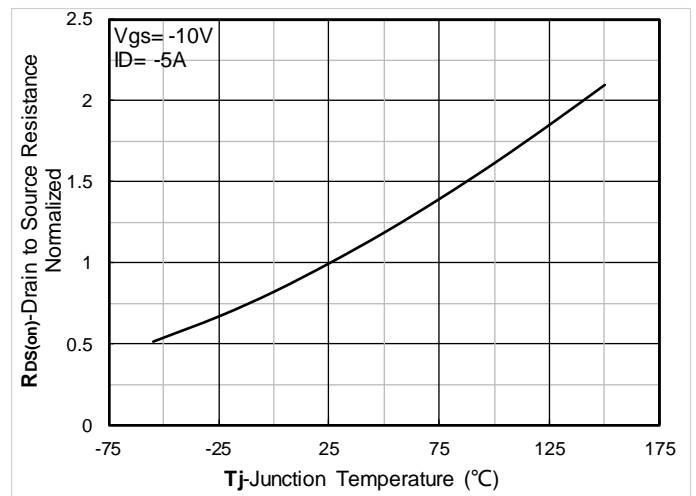


Figure 6. Normalized On-Resistance



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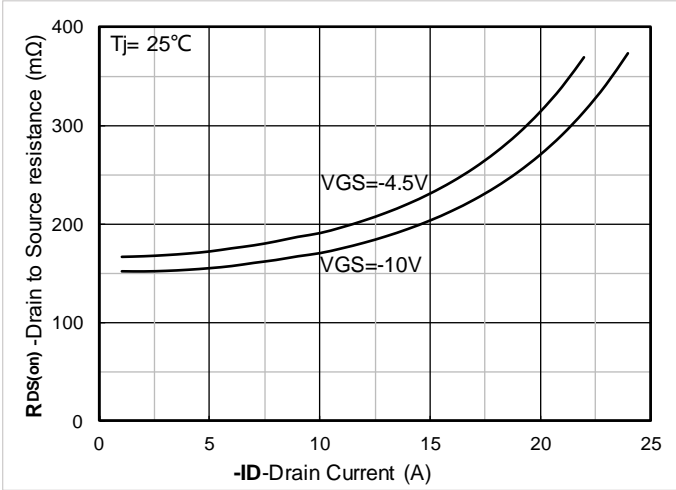


Figure 7.  $R_{DS(on)}$  VS Drain Current

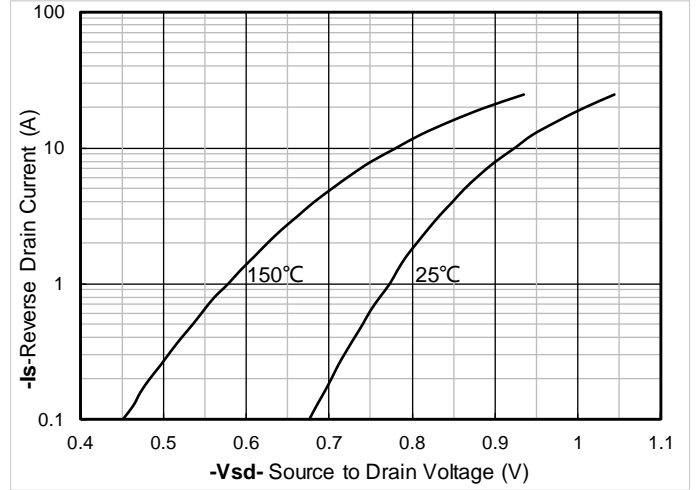


Figure 8. Forward characteristics of reverse diode

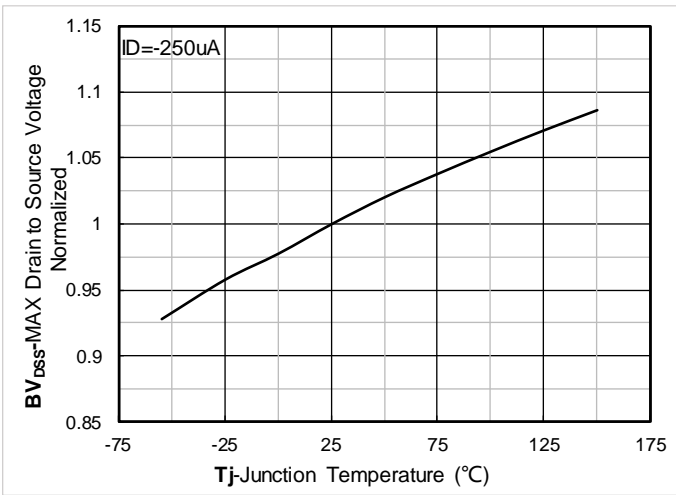


Figure 9. Normalized breakdown voltage

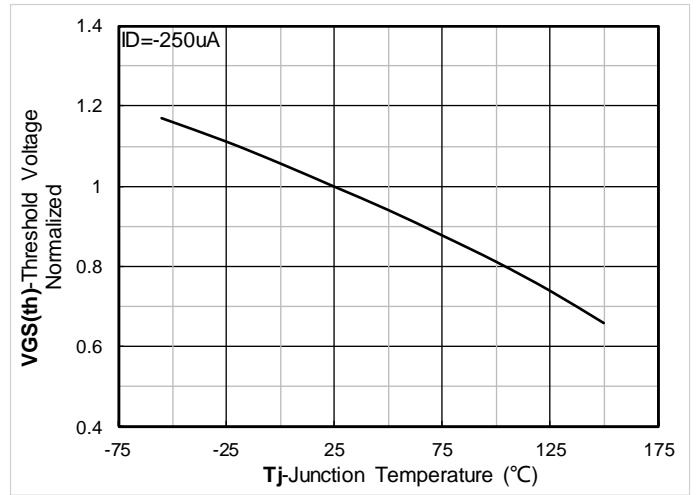


Figure 10. Normalized Threshold voltage

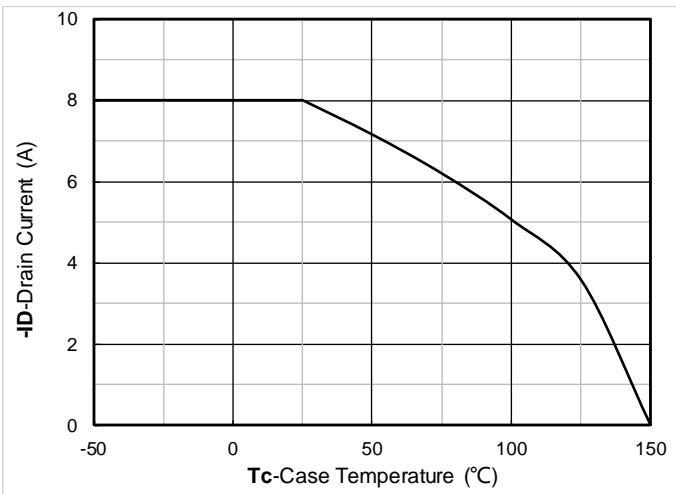


Figure 11. Current dissipation

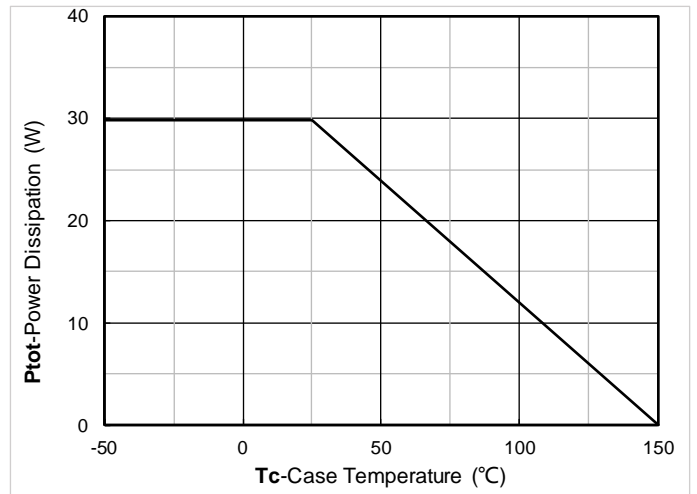


Figure 12. Power dissipation



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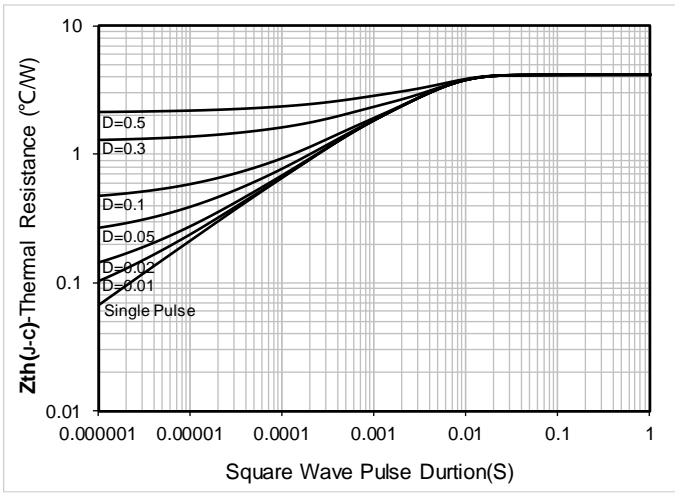


Figure 13. Maximum Transient Thermal Impedance

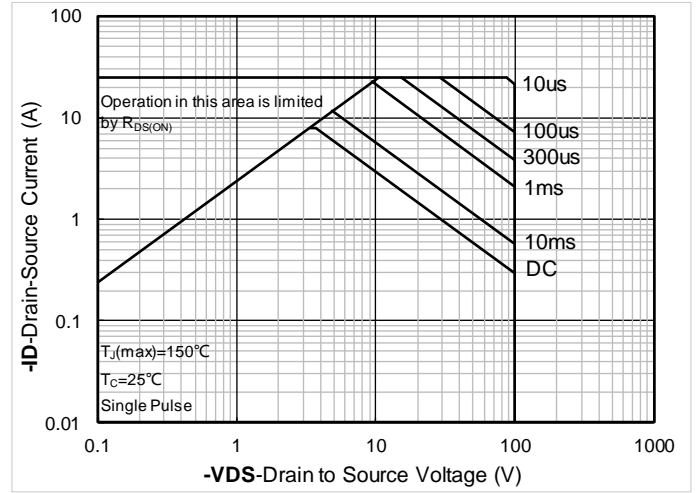
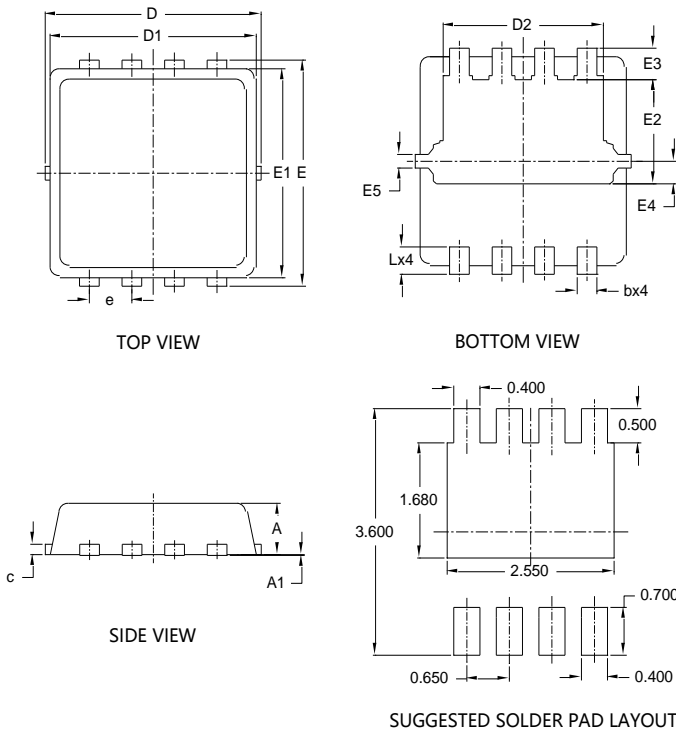


Figure 14. Safe Operation Area



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## ■ PDFN3333-8L-B-0.75MM Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.028	0.033	0.700	0.850
A1	0.000	0.002	0.000	0.050
b	0.008	0.016	0.200	0.400
c	0.004	0.010	0.100	0.250
D	0.124	0.136	3.150	3.450
D1	0.118	0.130	3.000	3.300
D2	0.089	0.104	2.250	2.650
E	0.124	0.136	3.150	3.450
E1	0.114	0.126	2.900	3.200
E2	0.052	0.068	1.320	1.720
E3	0.011	0.026	0.280	0.650
E4	0.013 REF		0.330 REF	
E5	0.008 REF		0.200 REF	
e	0.026 BSC		0.650 BSC	
L	0.012	0.020	0.300	0.500

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

UNIT: mm



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