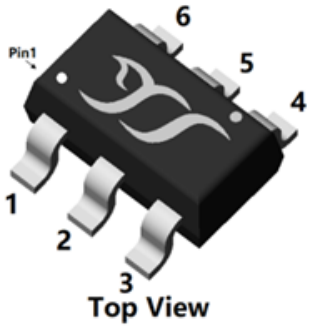
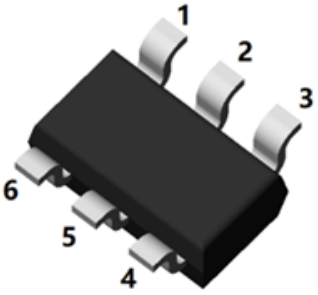
N-Channel and P-Channel Complementary Power MOSFET

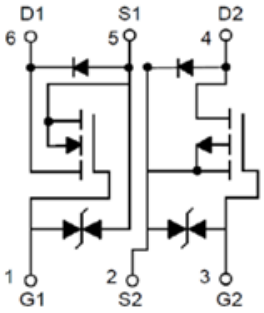


Top View



Bottom View

SOT-23-6L



Product Summary

NMOS(Die1)

- V_{DS} 20V
- I_D 0.5A
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜280 mohm
- $R_{DS(ON)}$(at V_{GS}=2.5V) ＜400 mohm
- ESD Protected Up to 2.0KV (HBM)

PMOS(Die2)

- V_{DS} -20V
- I_D -0.5A
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜850 mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜1200 mohm
- ESD Protected Up to 2.0KV (HBM)

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Interfacing, Logic switch
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	20	-20	V
Gate-source Voltage		V_{GS}	±12	±12	V
Drain Current	T_C=25℃	I_D	0.5	-0.5	A
	T_C=70℃		0.4	-0.4	
Pulsed Drain Current [A]		I_{DM}	2.3	-2.3	A
Total Power Dissipation	T_C=25℃	P_D	0.3	0.3	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]		$R_{\theta JA}$	416	416	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55~+150	-55~+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJJ3439KA	F2	49KA	3000	30000	120000	7“ reel

■ N-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V		±1.5	±10	μA
		V_{GS}= ±8V, V_{DS}=0V		±500	±2000	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	0.35	0.75	1.1	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 4.5V, I_D=0.5A		180	280	mΩ
		V_{GS}= 2.5V, I_D=0.3A		250	400	
		V_{GS}= 1.8V, I_D=0.2A		420	650	
Diode Forward Voltage [C]	V_{SD}	I_S=0.5A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				0.5	A
Dynamic Parameters [B]						
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		52		pF
Output Capacitance	C_{oss}			19		
Reverse Transfer Capacitance	C_{rss}			2.3		
Switching Parameters [B]						
Total Gate Charge	Q_g	V_{GS}=4.5V,V_{DS}=10V,I_D=0.5A		1		nC
Gate Source Charge	Q_{gs}			0.27		
Gate Drain Charge	Q_{gd}			0.21		
Reverse Recovery Charge	Q_{rr}	I_F=0.5A, di/dt=-20A/us		0.39		
Reverse Recovery Time	t_{rr}			14		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=10V,R_G=10Ω,I_D=500mA		2.1		
Turn-on Rise Time	t_r			17.5		
Turn-off Delay Time	$t_{D(off)}$			9.5		
Turn-off Fall Time	t_f			22		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ P-MOS Electrical Characteristics (TJ=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V		±1.5	±10	μA
		V_{GS}= ±8V, V_{DS}=0V		±500	±2000	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.35	-0.62	-1.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D=-0.5A		610	850	mΩ
		V_{GS}= -2.5V, I_D=-0.3A		930	1200	
		V_{GS}= -1.8V, I_D=-0.2A		1100	1700	
Diode Forward Voltage	V_{SD}	I_S=-0.5A,V_{GS}=0V			-1.2	V
Maximum Body-Diode Continuous Current	I_S				-0.5	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHZ		70		pF
Output Capacitance	C_{oss}			19		
Reverse Transfer Capacitance	C_{rss}			14		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DD}=-10V,I_D=-0.5A		1.22		nC
Gate Source Charge	Q_{gs}			0.36		
Gate Drain Charge	Q_{gd}			0.26		
Reverse Recovery Chrage	Q_{rr}	I_F=-0.5A, di/dt=-20A/us		0.95		
Reverse Recovery Time	t_{rr}			24		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, R_L=2.5Ω, R_{GEN}=3Ω		4.5		
Turn-on Rise Time	t_r			18		
Turn-off Delay Time	$t_{D(off)}$			15		
Turn-off Fall Time	t_f			23		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ N-MOS Typical Performance Characteristics

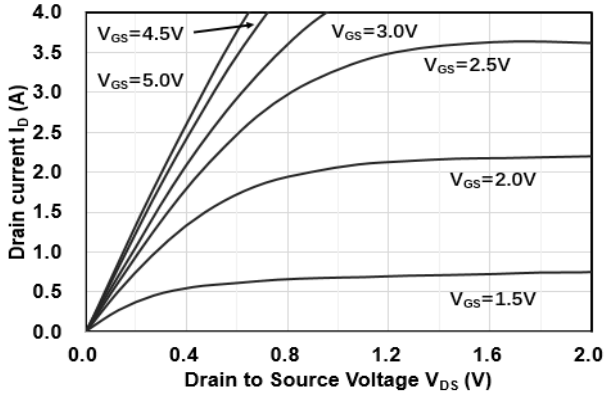


Figure1. Output Characteristics

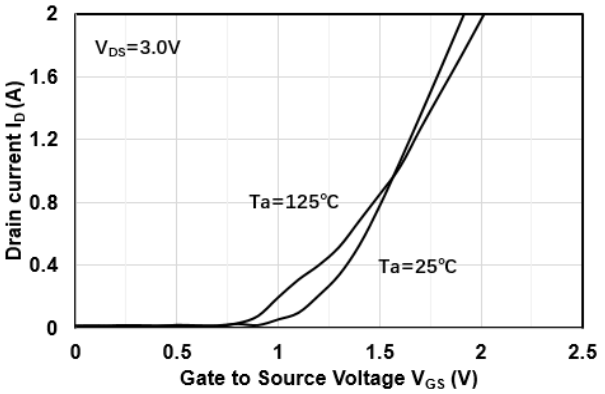


Figure2. Transfer Characteristics

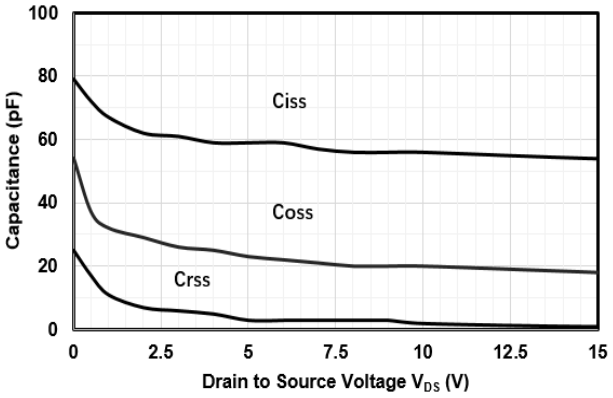


Figure3. Capacitance Characteristics

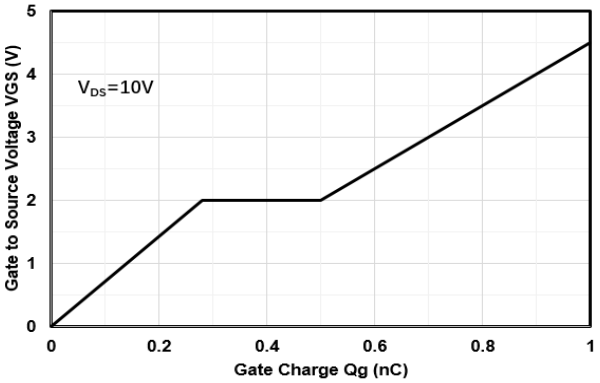


Figure4. Gate Charge

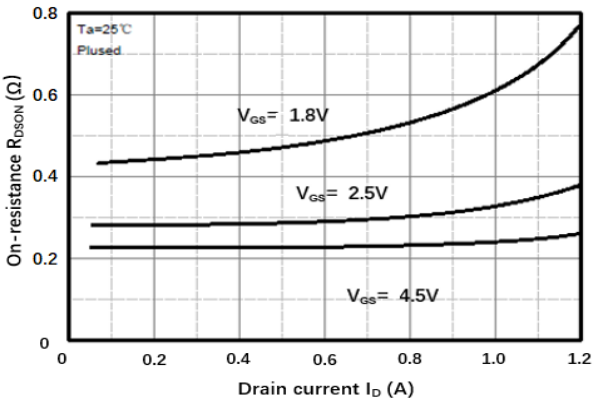


Figure5. Drain-Source on Resistance

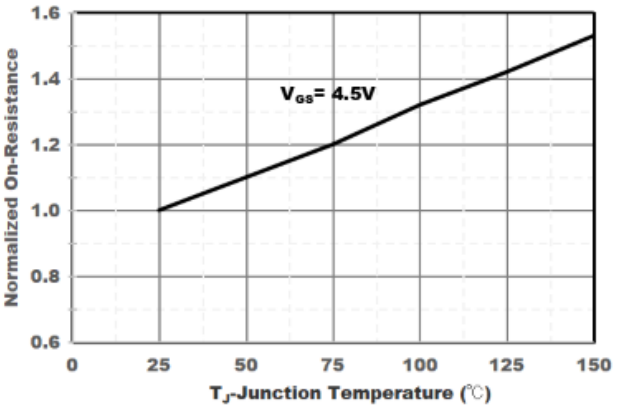


Figure6. Drain-Source on Resistance

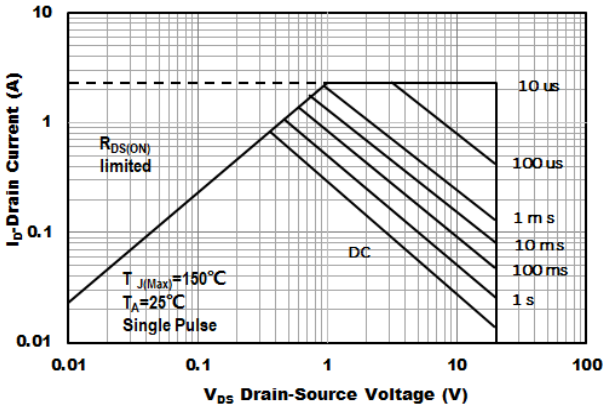


Figure7. Safe Operation Area

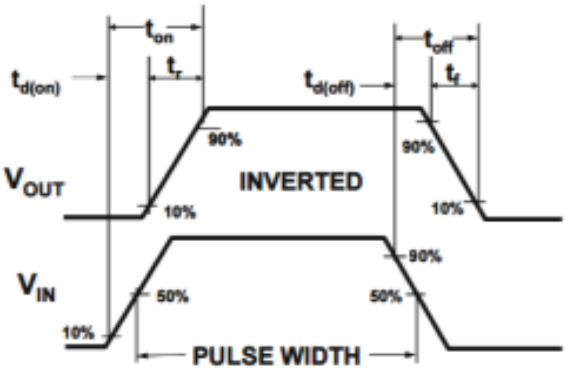


Figure8. Switching wave

■ P-MOS Typical Performance Characteristics

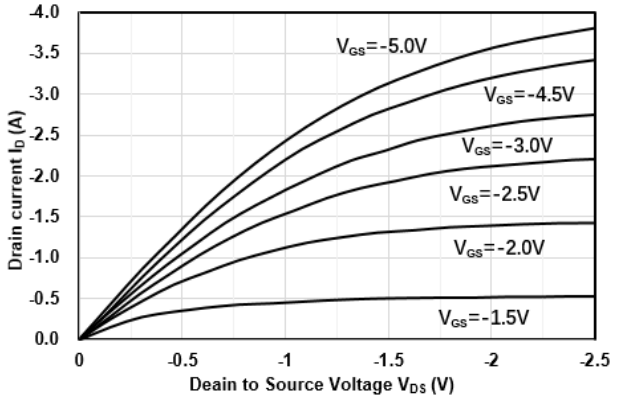


Figure1. Output Characteristics

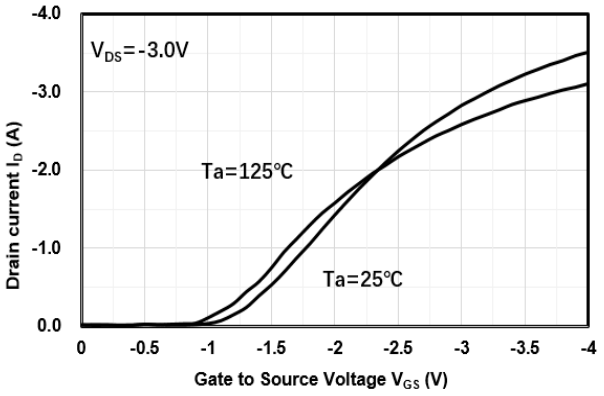


Figure2. Transfer Characteristics

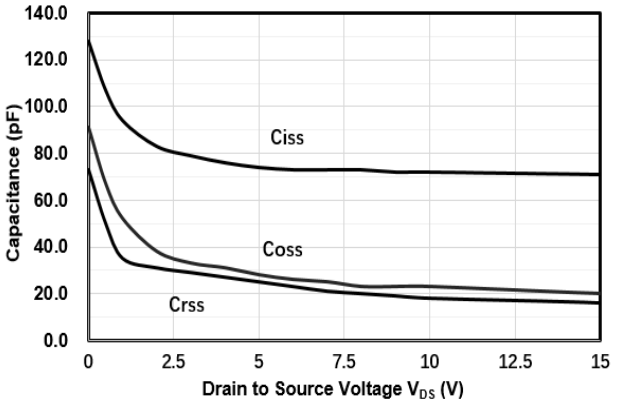


Figure3. Capacitance Characteristics

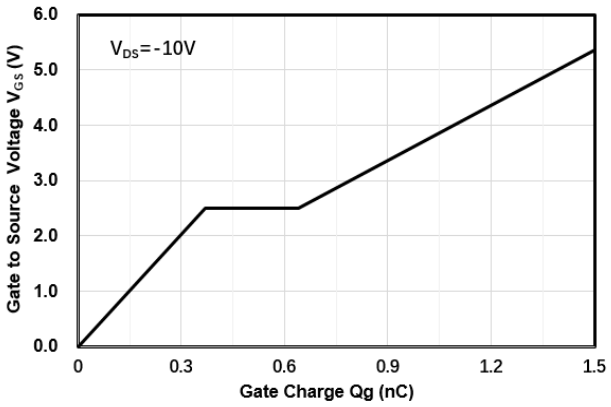


Figure4. Gate Charge

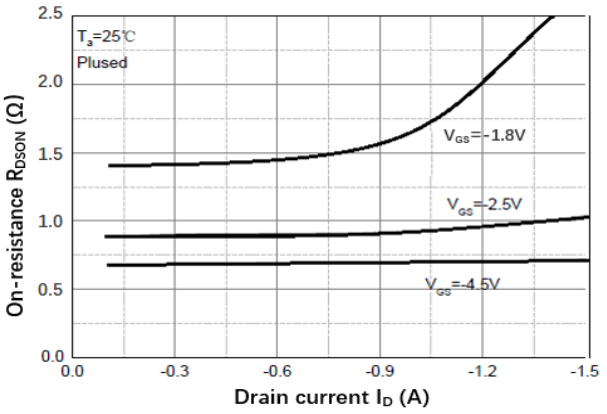


Figure5. Drain-Source on Resistance

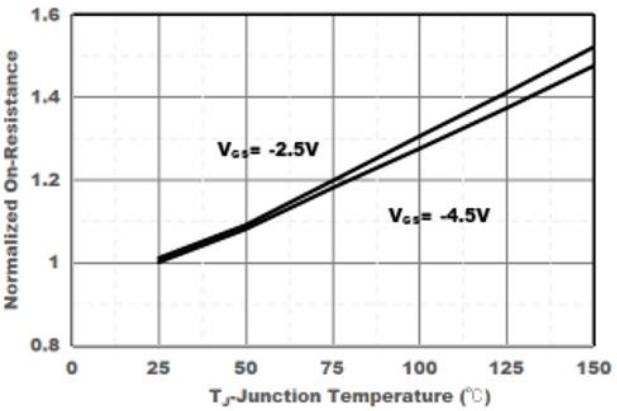


Figure6. Drain-Source on Resistance

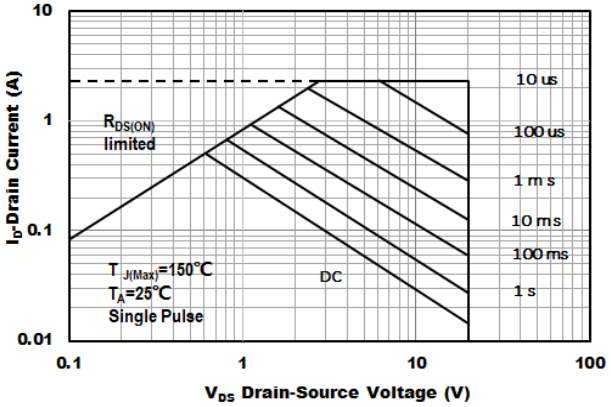


Figure7. Safe Operation Area

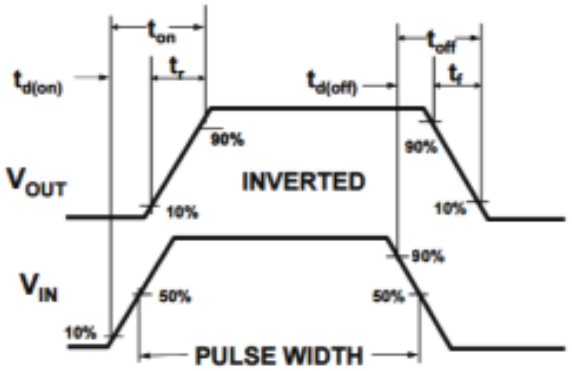
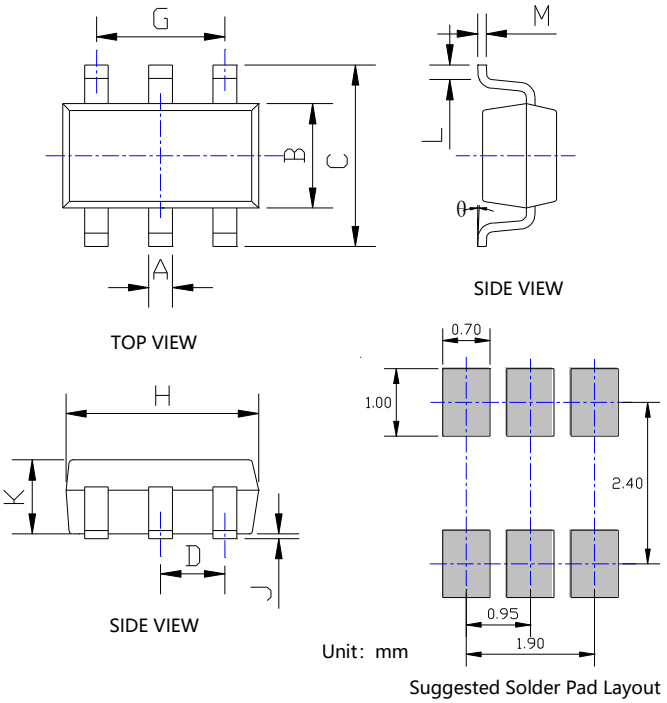


Figure8. Switching wave

■ SOT-23-6L Package Information



DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.012	0.020	0.300	0.500
B	0.059	0.067	1.500	1.700
C	0.104	0.116	2.650	2.950
D	0.037BSC		0.950BSC	
G	0.075BSC		1.900BSC	
H	0.111	0.119	2.820	3.020
J	0.000	0.004	0.000	0.100
K	0.041	0.045	1.050	1.150
L	0.012	0.024	0.300	0.600
M	0.004	0.008	0.100	0.200
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

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